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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,917	12/29/2003	Joseph M. Jeddeloh	501320.01 (30305/US)	6798

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EXAMINER	
BROWN, MICHAEL J	
ART UNIT	PAPER NUMBER
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/22/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/747,917	JEDDELOH ET AL.	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/29/06 and 12/8/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 9/29/2006 and 12/8/2006 were filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Leggige et al.(6,587,912).

As to claim 1, Leggige discloses a memory module(memory module 210a, see Fig. 3), comprising a plurality of memory devices(memory devices 301, see Fig. 3), and a memory hub(memory repeater hub 320, see Fig. 3), comprising a link interface(bus 300, see Fig. 3) receiving memory requests for access to at least one of the memory.

devices, and a memory device interface(bus 321, see Fig. 3) coupled to the memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests. Leggige also discloses the memory hub comprising a read synchronization module(clock buffer 716, address interface circuit 718, control interface circuit 719, data I/O circuit 722, and control logic 702, see Fig. 7) coupled to the memory device interface, the read synchronization module operable to compare timing between coupling read data from the memory devices and coupling read data from the memory hub and to generate an adjust signal corresponding to the compared timing, and a memory sequencer(control interface circuit 719 and control logic 702, see Fig. 7) coupled to the link interface, the memory device interface, and the read synchronization module, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to adjust the timing at which read memory requests are coupled to the memory device interface responsive to the adjust signal(see column 9, lines 18-22).

As to claim 2, Leggige discloses the memory module wherein the link interface comprises an optical input/output port(see column 1, lines 43-45).

As to claim 3, Leggige discloses the memory module wherein the read synchronization module comprises a buffer(read buffer 738, see Fig. 7) coupled to at least one memory device and the memory sequencer, the buffer operable to store received read data and to subsequently output the stored read data.

As to claim 4, Leggige discloses the memory module wherein the read synchronization module comprises a write pointer coupled to at least one memory device, the write pointer operable to increment in response to read data being stored in the buffer(see control logic 702, Fig. 7), a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the buffer(see control logic 702, Fig. 7), and a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing(see control logic 702, Fig. 7).

As to claim 5, Leggige discloses the memory module wherein the read synchronization module comprises a write pointer coupled to at least one memory device, the write pointer operable to increment in response to a read strobe coupled to the memory device(see control logic 702, Fig. 7), a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the memory module(see control logic 702, Fig. 7), and a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing(see control logic 702, Fig. 7).

As to claim 6, Leggige discloses the memory module wherein the memory devices comprise dynamic random access memory devices(see column 2, lines 26-28).

As to claim 7, Leggige discloses the memory module wherein the memory sequencer is operable to increase a period between receiving the memory requests

from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of a decrease in the timing between coupling read data from the memory devices and coupling read data from the memory hub, the memory sequencer further being operable to decrease the period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of an increase in the timing between coupling read data from the memory devices and coupling read data from the memory hub(see column 8, lines 18-28).

As to claim 8, Leggige discloses a memory module(memory module 210a, see Fig. 3), comprising a plurality of memory devices(memory devices 301, see Fig. 3), each of the memory devices being operable to output read data signals and a read data strobe signal responsive to respective memory requests, and a memory hub(memory repeater hub 320, see Fig. 3), comprising a link interface(bus 300, see Fig. 3) receiving memory requests for access to at least one of the memory devices, a memory device interface(bus 321, see Fig. 3) coupled to the memory devices, the memory device interface being operable to couple the received memory requests to at least one of the memory devices and to receive the read data signals and the read data strobe signal responsive to respective memory requests, and a buffer(read buffer 738, see Fig. 7) coupled to receive the read data signals, the read data signals being clocked into the buffer responsive to the read data strobe signal. Leggige also discloses the memory hub comprising a read synchronization module(clock buffer 716, address interface circuit 718, control interface circuit 719, data I/O circuit 722, and control logic 702, see

Fig. 7) coupled to the memory device interface, the read synchronization module operable to compare timing between the read data strobe signals and a core clock signal and to generate an adjust signal corresponding to the compared timing, and a memory sequencer(control interface circuit 719 and control logic 702, see Fig. 7) coupled to the link interface, the memory device interface, and the read synchronization module, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to adjust the timing at which read memory requests are coupled to the memory device interface responsive to the adjust signal(see column 9, lines 18-22).

As to claim 9, Leggige discloses the memory module wherein the link interface comprises an optical input/output port(see column 1, lines 43-45).

As to claim 10, Leggige discloses the memory module wherein the read data signals are clocked out of the buffer responsive to the core clock signal(see column 9, lines 18-22).

As to claim 11, Leggige discloses the memory module wherein the read synchronization module comprises a write pointer coupled to at least one memory device, the write pointer operable to increment in response to the read data strobe(see control logic 702, Fig. 7), a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to the core clock signal(see control logic 702, Fig. 7), and a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer

and to generate the adjust signal corresponding to the compared timing(see control logic 702, Fig. 7).

As to claim 12, Leggige discloses the memory module of claim 8 wherein the memory devices comprise dynamic random access memory devices(see column 2, lines 26-28).

As to claim 13, Leggige discloses a memory hub(memory repeater hub 320, see Fig. 3), comprising a link interface(bus 300, see Fig. 3) receiving memory requests for access to memory cells in at least one memory device(memory devices 301, see Fig. 3), and a memory device interface(bus 321, see Fig. 3) coupled to a plurality of memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests. Leggige also discloses the memory hub comprising a read synchronization module(clock buffer 716, address interface circuit 718, control interface circuit 719, data I/O circuit 722, and control logic 702, see Fig. 7) coupled to the memory device interface, the read synchronization module operable to compare timing between coupling read data from the memory devices and coupling read data from the memory hub and to generate an adjust signal corresponding to the compared timing, and a memory sequencer(control interface circuit 719 and control logic 702, see Fig. 7) coupled to the link interface, the memory device interface, and the read synchronization module, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being

operable to adjust the timing at which read memory requests are coupled to the memory device interface responsive to the adjust signal(see column 9, lines 18-22).

As to claim 14, Leggige discloses the memory hub wherein the link interface comprises an optical input/output port(see column 1, lines 43-45).

As to claim 15, Leggige discloses the memory hub wherein the read synchronization module comprises a buffer(read buffer 738, see Fig. 7) coupled to at least one memory device and the memory sequencer, the buffer operable to store received read data and to subsequently output the stored read data.

As to claim 16, Leggige discloses the memory hub wherein the read synchronization module comprises a write pointer coupled to at least one memory device, the write pointer operable to increment in response to read data being stored in the buffer(see control logic 702, Fig. 7), a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the buffer(see control logic 702, Fig. 7), and a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing(see control logic 702, Fig. 7).

As to claim 17, Leggige discloses the memory hub wherein the read synchronization module comprises a write pointer coupled to at least one memory device, the write pointer operable to increment in response to a read strobe coupled to the memory device(see control logic 702, Fig. 7), a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being

output from the memory hub(see control logic 702, Fig. 7), and a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing(see control logic 702, Fig. 7).

As to claim 18, Leggige discloses the memory hub wherein the memory devices comprise dynamic random access memory devices(see column 2, lines 26-28).

As to claim 19, Leggige discloses the memory hub wherein the memory sequencer is operable to increase a period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of a decrease in a period between the read pointer and the write pointer, the memory sequencer further being operable to decrease the period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of an increase in the period between the read pointer and the write pointer(see column 8, lines 18-28).

As to claim 20, Leggige discloses a computer system(computer system 100, see Fig. 1), comprising a central processing unit ("CPU")(processor 101, see Fig. 1), a system controller(bridge memory controller 111, see Fig. 3) coupled to the CPU, the system controller having an input port and an output port, an input device(keyboard interface 132, see Fig. 1) coupled to the CPU through the system controller, and an output device(audio controller 133, see Fig. 1) coupled to the CPU through the system controller, and a storage device(memory 113, see Fig. 1) coupled to the CPU through

the system controller. Leggige also discloses the computer system comprising a plurality of memory modules(memory modules 210a, 211a, 212a; see Fig. 3), each of the memory modules comprising a plurality of memory devices(memory devices 301, 302, 303, 304, 305, 306; see Fig. 3), and a memory hub(memory repeater hub 320, see Fig. 3), comprising a link interface(bus 300, see Fig. 3) receiving memory requests for access to at least one of the memory devices, and a memory device interface(bus 321, see Fig. 3) coupled to the memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests. Leggige further discloses the memory hub comprising a read synchronization module(clock buffer 716, address interface circuit 718, control interface circuit 719, data I/O circuit 722, and control logic 702, see Fig. 7) coupled to the memory device interface, the read synchronization module operable to compare timing between coupling read data from the memory devices and coupling read data from the memory hub and to generate an adjust signal corresponding to the compared timing, and a memory sequencer(control interface circuit 719 and control logic 702, see Fig. 7) coupled to the link interface, the memory device interface, and the read synchronization module, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to adjust the timing at which read memory requests are coupled to the memory device interface responsive to the adjust signal(see column 9, lines 18-22).

As to claim 21, Leggige discloses the computer system wherein the link interface comprises an optical input/output port(see column 1, lines 43-45).

As to claim 22, Leggige discloses the computer system wherein the read synchronization module comprises a buffer(read buffer 738, see Fig. 7) coupled to at least one memory device and the memory sequencer, the buffer operable to store received read data and to subsequently output the stored read data.

As to claim 23, Leggige discloses the computer system wherein the read synchronization module further comprises a write pointer coupled to at least one memory device, the write pointer operable to increment in response to read data being stored in the buffer(see control logic 702, Fig. 7), a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the buffer(see control logic 702, Fig. 7), and a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing(see control logic 702, Fig. 7).

As to claim 24, Leggige discloses the computer system wherein the read synchronization module further comprises a write pointer coupled to at least one memory device, the write pointer operable to increment in response to a read strobe coupled to the memory device(see control logic 702, Fig. 7), a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the memory module(see control logic 702, Fig. 7), and a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the

comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing(see control logic 702, Fig. 7).

As to claim 25, Leggige discloses the computer system wherein the memory devices comprise dynamic random access memory devices(see column 2, lines 26-28).

As to claim 26, Leggige discloses the computer system wherein the memory sequencer is operable to increase a period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of a decrease in the timing between coupling read data from the memory devices and coupling read data from the memory hub, the memory sequencer further being operable to decrease the period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of an increase in the timing between coupling read data from the memory devices and coupling read data from the memory hub(see column 8, lines 18-28).

As to claim 27, Leggige discloses a method of reading data from a memory module(memory module 210a, see Fig. 3), comprising receiving memory requests for access to a memory device(memory devices 301, see Fig. 3) in the memory module(bus 300, see Fig. 3), and coupling the memory requests to the memory device responsive to the received memory request, at least some of the memory requests being memory requests to read data(bus 321, see Fig. 3). Leggige also discloses the method comprising receiving read data responsive to the read memory requests, outputting the read data from the memory module(data I/O circuit 722, see Fig. 7), and

comparing timing between receiving the read data and outputting the read from the memory module(clock buffer 716, address interface circuit 718, control interface circuit 719, data I/O circuit 722, and control logic 702, see Fig. 7); and adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compared timing(control interface circuit 719 and control logic 702, see Fig. 7) (see column 9, lines 18-22).

As to claim 28, Leggige discloses the method further comprising storing the received read data in a buffer(read buffer 738, see Fig. 7).

As to claim 29, Leggige discloses the method wherein the buffer comprises a circular buffer(read buffer 738, data handling logic 746, write buffer 712, and data I/O circuit 722; see Fig. 7).

As to claim 30, Leggige discloses the method wherein the act of comparing the timing between receiving the read data and outputting the read from the memory module comprises incrementing a write pointer in response to receiving the read data(see control logic 702, Fig. 7), incrementing a read pointer in response to outputting the read data from the memory module(see control logic 702, Fig. 7), and comparing the write pointer to the read pointer(see control logic 702, Fig. 7).

As to claim 31, Leggige discloses the method wherein the act of receiving memory requests for access to a memory device mounted on the memory module comprises receiving optical signals corresponding to the memory requests(see column 8, lines 18-28).

As to claim 32, Leggige discloses the method wherein the act of adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compared timing comprises increasing a delay between receiving the memory requests and coupling the memory requests to the memory device responsive to a decrease in the period between receiving the read data and outputting the read from the memory module(see column 8, lines 18-28), and decreasing the delay between receiving the memory requests and coupling the memory requests to the memory device responsive to an increase in the period between receiving the read data and outputting the read from the memory module(see column 8, lines 18-28).

As to claim 33, Leggige discloses a method of coupling read data from a memory device(memory devices 301, see Fig. 3) to a buffer(read buffer 738, see Fig. 7) and outputting read data from the buffer, comprising coupling memory requests to the memory device, at least some of the memory requests being memory requests to read data(bus 321, see Fig. 3), and receiving read data responsive to the read memory requests(bus 300, see Fig. 3). Leggige also discloses the method comprises storing the received read data in the buffer, outputting the read data from the buffer(data I/O circuit 722, see Fig. 7), and comparing timing between storing the read data in the buffer and outputting the read from the buffer(clock buffer 716, address interface circuit 718, control interface circuit 719, data I/O circuit 722, and control logic 702, see Fig. 7), and adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compared timing(control interface circuit 719 and control logic 702, see Fig. 7) (see column 9, lines 18-22).

As to claim 34 Leggige discloses the method wherein the buffer comprises a circular buffer(read buffer 738, data handling logic 746, write buffer 712, and data I/O circuit 722; see Fig. 7).

As to claim 35, Leggige discloses the method wherein the act of comparing the timing between storing the read data in the buffer and outputting the read from the buffer comprises incrementing a write pointer in response to storing the read data in the buffer(see control logic 702, Fig. 7), incrementing a read pointer in response to outputting the read from the buffer(see control logic 702, Fig. 7), and comparing the write pointer to the read pointer(see control logic 702, Fig. 7).

As to claim 36, Leggige discloses the method wherein the act of adjusting the timing at which read memory requests are coupled to the memory device interface comprises increasing a delay in coupling the memory requests to the memory device responsive to a decrease in the period between the write pointer and the read pointer(see column 8, lines 18-28), and decreasing the delay in coupling the memory requests to the memory device responsive to an increase in the period between the write pointer and the read pointer(see column 8, lines 18-28).

Response to Arguments

3. Applicant's arguments, see Remarks, filed 10/4/2006, with respect to the rejection(s) of claim(s) 1-36 under Leggige et al.(6,587,912) have been fully considered

and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the same prior art, Leggige et al.(6,587,912).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Brown whose telephone number is (571)272-5932. The examiner can normally be reached on Monday-Thursday from 7:00am to 5:30pm(EST).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIRS) system. Status information for the published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications are available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
12/20/06